Sterne Kessler Goldstein Fox
ATTORNEYS AT LAW

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WRITER'S DIRECT NUMBER:
(202) 772-8550
INTERNET ADDRESS:
EKESSLER@SKGF.COM

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Art Unit 2111

Attn: Mail Stop Appeal Brief - Patents

Re: U.S. Utility Patent Application
Application No. 09/715,772; Filed: November 17, 2000
For: **Multi-Thread Peripheral Processing Using Dedicated Peripheral Bus**
Inventors: DENNIS *et al.*
Our Ref: 2222.4210001

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Supplemental Reply Brief Under 37 C.F.R. § 41.41; and

2. Return postcard.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Edward J. Kessler
Attorney for Applicants
Registration No. 25,688

EJK/SMB/k-d
Enclosures

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: DENNIS *et al.*	Confirmation No.: 7033
Application No.: 09/715,772	Art Unit: 2111
Filed: November 17, 2000	Examiner: Khanh Dang
For: **Multi-Thread Peripheral Processing Using Dedicated Peripheral Bus**	Atty. Docket: 2222.4210001

Supplemental Reply Brief Under 37 C.F.R. § 41.41

Mail Stop Appeal Brief - Patents

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PO Box 1450
Alexandria, VA 22313-1450

Sir:

Appellants filed a Brief on Appeal to the Board of Patent Appeals and Interferences for the above-captioned application on May 18, 2006, appealing the decision of the Examiner in the Final Office Action mailed July 19, 2005. The Examiner's Answer was mailed on July 31, 2006. Appellants submitted a Reply Brief Under 37 C.F.R. §41.41 on October 2, 2006. The Examiner mailed a Supplemental Examiner's Answer on December 8, 2006. Appellants submit this Supplemental Reply Brief under 37 C.F.R. §41.41 in response.

A. Rejection of claims 1-12, 14-25, 27-38, and 41 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,815,727 to Motomura

1. The Anticipation Rejection with Respect to Claims 1-7 and 10-12 is in Error and Must be Reversed

Appellants maintain their position that Motomura does not teach or suggest each feature of Appellants' independent claim 1. Appellants further disagree with the Examiner's interpretation of the present invention.

Independent claim 1 of the present invention recites "an apparatus" including:

> a peripheral bus coupled to a peripheral unit to transfer peripheral information including a command message specifying a peripheral operation; and
> a processing slice coupled to the peripheral bus to execute a plurality of threads comprising instructions, the plurality of threads including a first thread sending the command message to the peripheral unit;
> wherein the processing slice comprises a functional unit to perform a register operation specified in the instructions dispatched from each of the plurality of threads; and
> wherein the processing slice executes the instructions from more than one of the plurality of threads concurrently in a clock cycle.

The Examiner indicates in the Response to Reply Brief of the Supplemental Examiner's Answer that "it is clear that the term 'executed concurrently' does NOT mean that there is no 'wait state' or 'stalled' state between threads execution in Applicants' claimed invention," and adds that "the threads can be said to be 'executed concurrently, in a clock cycle'" only by virtue of "the use of 'waiting state' and 'stalled state' between threads execution." (Supplemental Examiner's Answer, p. 4). Appellants believe this to be a mischaracterization of the process by which a processing slice "executes the instructions from more than one of the plurality of threads concurrently in a clock cycle," as recited in claim 1.

Specifically, the Examiner states that "at the outset, it is acknowledged that Applicants concede that 'waiting state' is used in the claimed invention." (Supplemental Examiner's Answer, p. 4). Appellants do not concede that a "waiting state" is required in claim 1. The use of a "waiting state" is disclosed in the present Application, but it does not operate in the manner indicated by the Examiner. Specifically, the use of a "waiting state" is only relevant to the present invention in the context of the peripheral unit. (*see, e.g.,* Specification, p. 9, ll. 13-15; p. 11, ll. 9-12). A processing slice in the present

invention is operable to actually execute "the instructions from more than one of the plurality of threads concurrently in a clock cycle," as recited in claim 1, in a literal sense, rather than by time slicing, as the Examiner suggests. (*see* Supplemental Examiner's Answer, pp. 5-6). Furthermore, language in the present specification that the processing slices "includ[e] the ability to execute several instructions concurrently in the same clock cycle" finds support in the specification for a literal interpretation. (Specification, p. 8, ll. 23-25). During the execution of a peripheral operation (whether it is a "wait" or "no_wait" operation), instructions may be dispatched and processed concurrently, on a common clock cycle, from several threads to the register file 430, the condition code memory 440, the functional unit 450, or the memory access unit 460. (Specification, p. 10, ll. 21-25).

As recited in claim 1, the processing slice includes "a functional unit to perform a register operation" and is coupled to a peripheral unit. It is contemplated that more than one peripheral unit may be used. (Specification, p. 14, ll. 8-10). Even with a single peripheral unit, the present invention includes the ability to select "one or more instructions ... for execution concurrently" and blocks responsible for the concurrent processing "may terminate at the same time or at different times." (Specification, p. 14, ll. 12-17). Accordingly, while it may be the case that some of the blocks include peripheral access instructions that require a waiting state, a number of peripheral access instructions are, literally, processed simultaneously. *Id.* Each block is operable to perform, concurrent with other blocks, the tasks in FIG. 7. (Specification, p. 15, ll. 1-4).

Furthermore, instruction processing by the blocks is not limited to peripheral access instructions and includes non-message instructions. (Specification, p. 15, ll. 6-7). As previously noted, the concept of "waiting state" is only applicable to peripheral (i.e.

message) instructions. Accordingly, it is possible for the processing slice to "utilize functional and memory resources" concurrently with other resources, including peripheral unit access. (Specification, p. 15, ll. 18-20). For the reasons previously stated, and as agreed to by the Examiner, Motomura is unable to literally process multiple instructions "concurrently in a clock cycle" within a single processing slice as recited in claim 1, in the literal sense performed by the present invention. On the contrary, each processor in Motomura can execute only one thread at a time, and it is disclosed that each thread must go into a "waiting" or "completed" state before another thread is assigned to the processor. (Motomura, col. 8, ll. 40-51).

Since Motomura does not teach or suggest each and every feature of independent claim 1 it does not anticipate that claim. Accordingly, the Examiner's rejection of claim 1 must be reversed. Furthermore, dependent claims 2-7 and 10-12 are also not anticipated by Motomura for at least the same reasons as independent claim 1 from which they depend and further in view of their own respective features. Accordingly, the Examiner's rejection of claims 2-7 and 10-12 must also be reversed.

2. The Anticipation Rejection with Respect to Claims 14-20 and 23-25 is in Error and Must be Reversed

Appellants maintain their position that Motomura does not teach or suggest each feature of Appellants' claims 14-20 and 23-25. Appellants submit that claims 14-20 and 23-25 are distinguishable over Motomura for the additional reasons provided with respect to independent claim 1 in this Supplemental Reply Brief.

3. The Anticipation Rejection with Respect to Claims 27-33 and 36-38 is in Error and Must be Reversed

Appellants maintain their position that Motomura does not teach or suggest each feature of Appellants' claims 27-33 and 36-38. Appellants submit that claims 27-33 and

36-38 are distinguishable over Motomura for the additional reasons provided with respect to independent claim 1 in this Supplemental Reply Brief.

4. The Anticipation Rejection with Respect to Claim 41 is in Error and Must be Reversed

Appellants maintain their position that Motomura does not teach or suggest each feature of Appellants' claim 41. Appellants submit that claim 41 is distinguishable over Motomura for the additional reasons provided with respect to independent claim 1 in this Supplemental Reply Brief.

5. The Anticipation Rejection with Respect to Claims 8 and 9 is in Error and Must be Reversed

Appellants maintain their position that Motomura does not teach or suggest each feature of Appellants' claims 8 and 9. Appellants submit that claims 8 and 9 are distinguishable over Motomura for the additional reasons provided with respect to independent claim 1, from which they depend, in this Supplemental Reply Brief.

6. The Anticipation Rejection with Respect to Claims 21 and 22 is in Error and Must be Reversed

Appellants maintain their position that Motomura does not teach or suggest each feature of Appellants' claims 21 and 22. Appellants submit that claims 21 and 22 are distinguishable over Motomura for the additional reasons provided with respect to claims 8 and 9 in this Supplemental Reply Brief.

7. The Anticipation Rejection with Respect to Claims 34 and 35 is in Error and Must be Reversed

Appellants maintain their position that Motomura does not teach or suggest each feature of Appellants' claims 34 and 35. Appellants submit that claims 34 and 35 are

distinguishable over Motomura for the additional reasons provided with respect to claims 8 and 9 in this Supplemental Reply Brief.

B. Rejection of claims 13, 26, and 39 under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 5,815,727 to Motomura in view of U.S. Patent No. 5,418,917 to Hiraoka et al.

Appellants maintain their position that the combination of Motomura and Hiraoka does not teach or suggest each feature of Appellants' claims 13, 26, and 39.

C. Rejection of claim 40 under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 5,815,727 to Motomura in view of U.S. Patent No. 5,938,765 to Dove et al.

Appellants maintain their position that the combination of Motomura and Dove does not teach or suggest each feature of Appellants' claim 40.

D. Conclusion

In light of the arguments above, as well as those set forth in Appellants' Brief on Appeal filed May 18, 2006 and Appellants' Reply Brief filed October 2, 2006, Appellants respectfully submit that the final rejections of claims 1-41 are improper and should be reversed.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Edward J. Kessler
Attorney for Applicants
Registration No. 25,688

Date: 8 Feb. 2007

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600